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WHAT IS CLAIMED IS:

1. For use in a CDMA receiver, a noise reduction circuit for improving a signal-to-noise ratio of a received signal comprising a series of chip sequences, said noise reduction circuit comprising:

a sampling circuit capable of generating an original plurality of samples of said received signal; and

a controller capable of determining a first plurality of time slots, each of said first plurality of time slots comprising a plurality of chip samples corresponding to Logic 1, and a second plurality of time slots, each of said second plurality of time slots comprising a plurality of chip samples corresponding to Logic 0, wherein said controller is capable of generating a reconstructed plurality of samples by at least one of:

modifying an order of a first Logic 1 chip sample and a second Logic 1 chip sample; and

modifying an order of a first Logic 0 chip sample and a second Logic 0 chip sample.

2. The noise reduction circuit set forth in Claim 1 wherein said controller adds said reconstructed plurality of samples and said original plurality of samples to generate a composite signal having a reduced signal-to-noise ratio.

3. The noise reduction circuit set forth in Claim 1 wherein said CDMA receiver is a receiver in a base station of a wireless network.

4. The noise reduction circuit set forth in Claim 1 wherein said CDMA receiver is a receiver in a mobile station capable of communicating with a wireless network.

5. The noise reduction circuit set forth in Claim 1 wherein said first Logic 1 chip sample and said second Logic 1 chip sample are contained within a single chip.

6. The noise reduction circuit set forth in Claim 1 wherein said first Logic 0 chip sample and said second Logic 0 chip sample are contained within a single chip.

7. The noise reduction circuit set forth in Claim 1 wherein said first Logic 1 chip sample and said second Logic 1 chip sample are contained within different chips and said first Logic 0 chip sample and said second Logic 0 chip sample are contained within different chips.

8. The noise reduction circuit set forth in Claim 1 wherein said controller one of modifies said order of said first and second Logic 1 chip samples and modifies said order of said first and second Logic 0 chip samples according to one of a random process algorithm and a predetermined algorithm.

9. A CDMA wireless network comprising a plurality of base stations, each of said base stations comprising a noise reduction circuit for improving a signal-to-noise ratio of a received signal comprising a series of chip sequences, said noise reduction circuit comprising:

a sampling circuit capable of generating an original plurality of samples of said received signal; and

a controller capable of determining a first plurality of time slots, each of said first plurality of time slots comprising a plurality of chip samples corresponding to Logic 1, and a second plurality of time slots, each of said second plurality of time slots comprising a plurality of chip samples corresponding to Logic 0, wherein said controller is capable of generating a reconstructed plurality of samples by at least one of:

modifying an order of a first Logic 1 chip sample and a second Logic 1 chip sample; and

modifying an order of a first Logic 0 chip sample and a second Logic 0 chip sample.

10. The CDMA wireless network set forth in Claim 9 wherein said controller adds said reconstructed plurality of samples and said original plurality of samples to generate a composite signal having a reduced signal-to-noise ratio.

11. The CDMA wireless network set forth in Claim 9 wherein said first Logic 1 chip sample and said second Logic 1 chip sample are contained within a single chip.

12. The CDMA wireless network set forth in Claim 9 wherein said first Logic 0 chip sample and said second Logic 0 chip sample are contained within a single chip.

13. The CDMA wireless network set forth in Claim 9 wherein said first Logic 1 chip sample and said second Logic 1 chip sample are contained within different chips and said first Logic 0 chip sample and said second Logic 0 chip sample are contained within different chips.

14. The CDMA wireless network set forth in Claim 9 wherein said controller one of modifies said order of said first and second Logic 1 chip samples and modifies said order of said first and second Logic 0 chip samples according to one of a random process algorithm and a predetermined algorithm.

15. A wireless mobile station capable of communicating with a plurality of base stations in a wireless network, said wireless mobile station comprising a reduction circuit for improving a signal-to-noise ratio of a received signal comprising a series of chip sequences, said noise reduction circuit comprising:

a sampling circuit capable of generating an original plurality of samples of said received signal; and

a controller capable of determining a first plurality of time slots, each of said first plurality of time slots comprising a plurality of chip samples corresponding to Logic 1, and a second plurality of time slots, each of said second plurality of time slots comprising a plurality of chip samples corresponding to Logic 0, wherein said controller is capable of generating a reconstructed plurality of samples by at least one of:

modifying an order of a first Logic 1 chip sample and a second Logic 1 chip sample; and

modifying an order of a first Logic 0 chip sample and a second Logic 0 chip sample.

16. The wireless mobile station set forth in Claim 15 wherein said controller adds said reconstructed plurality of samples and said original plurality of samples to generate a composite signal having a reduced signal-to-noise ratio.

17. The wireless mobile station set forth in Claim 15 wherein said first Logic 1 chip sample and said second Logic 1 chip sample are contained within a single chip.

18. The wireless mobile station set forth in Claim 15 wherein said first Logic 0 chip sample and said second Logic 0 chip sample are contained within a single chip.

19. The wireless mobile station set forth in Claim 15 wherein said first Logic 1 chip sample and said second Logic 1 chip sample are contained within different chips and said first Logic 0 chip sample and said second Logic 0 chip sample are contained within different chips.

20. The wireless mobile station set forth in Claim 15 wherein said controller one of modifies said order of said first and second Logic 1 chip samples and modifies said order of said first and second Logic 0 chip samples according to one of a random process algorithm and a predetermined algorithm.

21. For use in a CDMA receiver, a method of improving a signal-to-noise ratio of a received signal comprising a series of chip sequences, the method comprising the steps of:

sampling the receiving signal to generate an original plurality of samples of the received signal;

determining a first plurality of time slots, each of the first plurality of time slots comprising a plurality of chip samples corresponding to Logic 1, and a second plurality of time slots, each of the second plurality of time slots comprising a plurality of chip samples corresponding to Logic 0; and

generating a reconstructed plurality of samples by at least one of:

modifying an order of a first Logic 1 chip sample and a second Logic 1 chip sample; and

modifying an order of a first Logic 0 chip sample and a second Logic 0 chip sample.

22. The method set forth in Claim 21 including the further step of adding the reconstructed plurality of samples and the original plurality of samples to generate a composite signal having a reduced signal-to-noise ratio.

23. The method set forth in Claim 21 wherein the first Logic 1 chip sample and the second Logic 1 chip sample are contained within a single chip.

24. The method set forth in Claim 21 wherein the first Logic 0 chip sample and the second Logic 0 chip sample are contained within a single chip.

25. The method set forth in Claim 21 wherein the first Logic 1 chip sample and the second Logic 1 chip sample are contained within different chips and the first Logic 0 chip sample and the second Logic 0 chip sample are contained within different chips.

26. The method set forth in Claim 1 wherein the sub-step of modifying the order of the first and second Logic 1 chip samples and the sub-step of modifying the order of the first and second Logic 0 chip samples are performed according to one of a random process algorithm and a predetermined algorithm.